CLAIMS

1. Circuitry for processing images and video, comprising:

a random access memory;

a motion estimation hardware accelerator coupled to said random access memory;

a transform coding hardware accelerator coupled to said random access memory; and

a processor coupling said hardware accelerators to said random access memory for executing software instructions for processing images and video, wherein some of the instructions initiate functions performed by one or more of said hardware accelerators.

2. The circuitry of claim 1 and further comprising a pixel interpolation hardware accelerator coupled to said random access memory.

3. The circuitry of claim 2 wherein said pixel interpolation hardware accelerator performs a half-pixel interpolation function.

4. The circuitry of claim 1 wherein said motion estimation hardware accelerator includes circuitry for calculating a mean absolute difference function.

5. The circuitry of claim 1 wherein said transform coding hardware accelerator includes circuitry for calculating a direct cosine transform function.

6. The circuitry of claim 5 wherein said transform coding hardware accelerator includes circuitry for calculating an inverse direct cosine transform function.

7. A method of processing video information, comprising the steps of:

executing a compression task in a programmable processing device coupled to a random access memory;

upon encountering a motion estimation instruction, initiating execution of an associated function in a motion estimation hardware accelerator, said motion estimation hardware accelerator coupled to said processing device and said random access memory; and

upon encountering a transform coding instruction, initiating execution of an associated function in a transform coding hardware accelerator, said transform coding hardware accelerator coupled to said processing device and said random access memory.

8. The method of claim 7 step of initiating execution of an associated function in the motion estimation hardware accelerator includes the step of retrieving image data from said random access memory into said motion estimation hardware accelerator.

9. The method of claim 7 step of initiating execution of an associated function in the transform coding hardware accelerator includes the step of retrieving image data from said random access memory into said transform coding hardware accelerator.

10. The method of claim 7 and further comprising the step of, upon encountering a pixel interpolation instruction, initiating execution of an associated function in a pixel interpolation hardware accelerator, said pixel interpolation hardware accelerator coupled to said processing device and said random access memory.

11. The method of claim 10 wherein said step of initiating execution of an associated function in a pixel interpolation hardware accelerator includes the step of performing a half-pixel interpolation function.

12. The method of claim 7 wherein said step of initiating execution of an associated function in a motion estimation hardware accelerator includes the step of performing a mean absolute difference function.

13. The method of claim 7 wherein said step of initiating execution of an associated function in a transform coding hardware accelerator includes the step of performing a direct cosine transform function.

14. The method of claim 13 wherein said step of initiating execution of an associated function in a transform coding hardware accelerator includes the step of performing an inverse direct cosine transform function.